GENERAL REMARKS:

Office Action C included a drawing objection as well as claim rejections and objections in two categories.

- **Drawing objections and 35 U.S.C. 112 second paragraph rejection of claim 19**

With regard to the drawing objection, Office Action C indicated that the drawings lacked a "means for allowing [a first photodetector (formerly sensor) output to change]" cited in claim **19**. Office Action C also rejected claim **19** under 35 U.S.C. 112 second paragraph as being indefinite, on grounds of the "means for allowing" being a function of "a first sensor" which Office Action C asserted was described on page 9, lines 14-19 of the Application's specification.

- **Summary of Applicant's response to drawing objections and 35 U.S.C. 112 rejection of claim 19**

The element cited as missing in the figures is in fact depicted in every figure, is thoroughly discussed in the specification, and would be clearly understood by one skilled in the art. However, the "means for allowing" the photodetector output to change is in fact the same as another element in claim **19**, a "means for initializing" the photodetector output. Per the suggestion of Office Action C, Applicant has removed the "means for allowing" element from claim **19** and has made no changes to the Application's figures.

Note in the paragraph above the change from the former "sensor output" to "photodetector output", which will be discussed below.

- **35 U.S.C. 102(e) rejection of claims 2-5 and 7-20 as anticipated by Laflaquiere**

Claims **2-5** and **7-20** were rejected in Office Action C under 35 U.S.C. 102(e) as anticipated by U.S. Patent 6,850,176 issued to Laflaquiere et al. Office Action C also objected to claim **6**, a dependent claim of claims **4, 3,** and **2**, but indicated it to be

allowable pending re-writing in independent form with all the limitations of its parent claims.

- **Summary of Applicant's response to 35 U.S.C. 102(e) rejections**

Laflaquiere is a difficult piece of prior art to read. Laflaquiere's claims contain ambiguous element references and describe a different invention than is described in Laflaquiere's specification. Laflaquiere's specification has technical analysis that is incorrect, fails to discuss or identify some important elements of the proposed invention, identifies other elements inconsistently, and includes substantial unclear and conflicting language. Moreover, Laflaquiere's figures are also inconsistent and in error.

Notwithstanding Laflaquiere's severe deficiencies, its contents do amount to prior art.

After careful consideration, Applicant has determined that there are two principal reasons for the 35 U.S.C. 102(e) rejections, one linguistic and the other technical.

- Clarification of "sensor"

The linguistic issue is determination of a reasonable definition of the term "sensor". In the Application, "sensor" has a relatively narrow definition, the context being "CMOS image sensor arrays" (e.g. page 1, line 23). In CMOS image sensor arrays, the sensors are photodetectors such as photodiodes. With additional supporting circuitry such as resetting devices, bus access transistors, and local amplifiers, the sensors become part of sensor cells. In turn, the sensor cells are grouped together to form arrays. Well-known sensor cell structures for CMOS image sensor arrays include the CMOS Active Pixel Sensor (APS) cell discussed in the specification and passive pixels, which lack amplifying transistor 28 of Application Fig. 2A.

However, in Laflaquiere, "sensor" is a a term with multiple different and conflicting scopes, as discussed later. In Office Action C, "sensor" has a fluid, liberal definition at odds with Laflaquiere's multiple definitions and also at adds with the scope of "sensor" presented in the Application's figures, specification, and claims.

Applicant has addressed the linguistic problem of defining "sensor" by using the narrower and more-well-defined term "photodetector" instead of the problematic "sensor". This is in keeping with the original intent of the Application and avoids the issues of broad interpretations of "sensor" from the prior art. In the claims, the word "sensor" is replaced by the word "photodetector". Applicant has also amended the specification on page 1 under BACKGROUND – FIELD OF THE INVENTION to clarify that in CMOS image sensor arrays, the sensors are photodetectors, and has amended the paragraph under SUMMARY on page 6 similarly. Discussion of the figures on page 9, lines 8-13 is amended to identify that in the figures, the element "photodiode 10" is the "photodetector" of the claims. The heading on page 13, line 23 is amended to properly refer to a "CMOS Active Pixel Sensor cell", while the paragraph of page 17, lines 11-16 is amended to correctly state that "digital count signals are provided to the sensor cells in the array".

- An appropriate treatment of Laflaquiere's processing circuitry is needed.

The technical reason for the 35 U.S.C. 102(e) rejections seems to be a misinterpretation of the nature and function of transistors 31 and 32 in Laflaquiere Fig. 6. Office Action C asserts that these transistors "couple" the signal at node 35 to the gates of transistors 33 and 34.

In fact, transistors 31 and 32 do NOT simply "couple" the signal at node 35 to the gates of transistors 33 and 34. They have a configuration similar to an AC small-signal amplifier, but the voltage at node 35 is not an AC small signal. It can swing from Vr all the way down to ground, and may do so slowly. The signal at the drain of transistor 31 is NOT the signal at node 35. Rather, it is monotonic, nonlinear function of the signal at node 35.

In contrast, the Application claims all clearly recite a limitation of the sensor output – not a monotonic, nonlinear function of the sensor output – applied to the transistor gates.

Applicant therefore submits that Laflaquiere fails to have or suggest ALL of the limitations of any of the claims rejected under 35 U.S.C. 102(e). For rejected independent claims **2**, **7**, **9**, and **11-13** the missing limitation is the element "means for

applying said first analog input to said first gate and to said second gate" recited in part b-iii of each. For independent claim **14**, the missing limitations are those defined by part a-i and by part b. For independent claim **19**, the missing limitations are part c (formerly part d) and part d (formerly part e), for part d particularly parts d-iv and d-v.

With this in mind, Applicant requests withdrawal of all the 35 U.S.C. 102(e) claim rejections and submits that claims **2-20** are in condition for allowance.

- **Summary of General Remarks**

With this Amendment, Applicant has addressed Office Action C drawing objections, 35 U.S.C. 112 second paragraph rejection of claim **19**, and 35 U.S.C. 102(e) rejections of claims **2-5** and **7-20**. The claims and specification have been amended in keeping with the original intent and scope of the Application to make the invention clear and well-defined as novel, unobvious, and useful. Applicant submits that all the claims are now in condition for allowance, and respectfully requests same.

Detailed discussions of the material in this General Remarks section appear in the remainder of this Amendment.

DRAWINGS:

Office Action C page 2 objected to the drawings under 37 CFR 1.83(a) as not showing the "means for allowing said first sensor output to change in response to incident energy" of Applicant's claim **19**, requiring either that the means be shown or that the element be removed from the claim.

In all of the figures of the Application, an element meeting the criterion is shown. In Figs. 1A, 1B, 1C, and 1E, the element is the labeled "reset transistor 14". "Reset transistor 14" is also shown in the prior art CMOS APS cell of Fig. 2A. In Fig. 1D, the element is the labeled "p-type reset transistor 34". In Fig. 2B, multiple instances of a circuit corresponding to Fig. 1E are depicted, though of course other embodiments are also possible.

It is clear to one skilled in the art that when reset transistor 14 (or p-type reset transistor 34) is on – i.e. conducting – the associated photodiode is connected to reset reference bus 16 (for Figs. 1A-1E) or to positive power supply bus 18 (for Fig. 2A). This resets or initializes the voltage across the photodiode AND prevents the voltage across the photodiode from changing in response to incident radiation. It is also clear that when the reset transistor 14 (or p-type reset transistor 34) is off – i.e. not conducting – the voltage across the photodiode can change in response to incident radiation. This is discussed on page 9, lines 14-19, cited by Office Action C in rejecting claim **19** under 35 U.S.C. 112.

Per the suggestion of Office Action C, Applicant has canceled the "means for allowing said first sensor output to change in response to incident energy" from claim **19**, and is keeping the drawings as they are.

CLAIM REJECTIONS – 35 U.S.C. 112:

Office Action C rejected Application claim **19** under 35 U.S.C. 112 as being indefinite, noting particularly the following:

> In claim 19, "means for allowing said first sensor output to change in response to incident energy" appears to be a function of "a first sensor" as described on lines 14-19 on page 9 of the specification instead of a separate and distinctive means.

Applicant first notes that Office Action C's reference is confusing. A keyword search for "first sensor" in the original application yields results only in claims and in the first full paragraph on page 16, lines 5-10, quoted below (underlining by Applicant):

> Further cost reductions may be possible from combining threshold detectors. For instance, a digital logic gate computing ((A AND S1) OR (NOT(A) AND S2)) could have A being a control signal determining whether the threshold detector output indicates the state of a <u>first sensor</u> output S1 or the state of a second sensor output S2. Of course, the detector would need to be accessed twice per elapsed time count value.

Lines 14-19 on page 9 of the specification read as follows:

> In actual operation, reset transistor 14 is switched on to pull the voltage across photodiode 10 up to the voltage on reset reference bus 16. Reset transistor 14 is then switched off and photodiode 10 is exposed to incident energy. Photo-generation of electron-hole pairs causes the voltage across photodiode 10 to change. The change is proportional to the cumulative incident energy. In other words, photodiode 10 acts as an integrator.

Note that the paragraph just above contains no mention of the phrase "first sensor".

The principal reason for Office Action C 35 USC 112 rejection of claim **19** appears to be that, as discussed above with respect to the drawings, the reset transistor in a sensor cell performs both initialization or reset (when it is ON) and allowing the sensor output to

change in response to incident radiation (such change not allowed with the reset transistor ON, such change allowed with the reset transistor OFF). Office Action C seems to assert that the "means for resetting" and the "means for allowing to change in response to incident energy" must be accomplished by separate elements in the specification and figures if they are listed as separate elements in the claim.

Applicant has therefore, as mentioned above with respect to the drawings, removed the element "means for allowing said first sensor output to change in response to incident energy" from claim **19**.

Applicant submits that claim **19** is now in condition for allowance and requests withdrawal of rejection under 35 U.S.C. 112.

CLAIM REJECTIONS – 35 U.S.C. 102:

Office Action C rejected claims **2-5** and **7-20** – that is to say, all but one of the claims – as anticipated by the prior art of U.S. Patent 6,850,176, also known as "Laflaquiere".

In this next section of this Amendment C, Applicant will analyze the content of Laflaquiere, demonstrating the following:

- Laflaquiere has no valid claims.
- Laflaquiere's figures contain several basic errors and are therefore unreliable.
- Laflaquiere's specification contains multiple, conflicting definitions of some terms, fails to explain other terms, and has incorrect analysis, making it, too, unreliable.

Altogether, the flaws in Laflaquiere suggest the authors did not have a deep and thorough understanding of the idea they were attempting to patent, an idea which should not have become a U.S. patent as issued.

On this basis, Applicant submits that a very strict and narrow interpretation of Laflaquiere is in order.

Following the extended discussion of the problems with Laflaquiere, Applicant will address the specific Office Action C discussion relating to Application claims rejected under 35 U.S.C. 102.

It is worth noting again – as mentioned in the General Remarks section above – that Office Action C claim rejections under 35 U.S.C. 102(e) rely on an incorrect interpretation that, with reference to Laflaquiere Fig. 6, transistors 31 and 32 are equivalent to Applicant's claim element "means for applying said first analog output to said first gate and said second gate", with the "first analog output" being the photodetector output (formerly "sensor" output – see discussion of drawing objections and 35 U.S.C. 112 rejection above) and the "first gate" and "second gate" being of transistors in a threshold detector.

Analysis and Discussion of Laflaquiere

- **Laflaquiere background**

"Laflaquiere" is prior art U.S. Patent 6,850,176, entitled METHOD FOR CONVERTING AN ANALOG SIGNAL INTO A DIGITAL SIGNAL AND ELECTROMAGNETIC RADIATION SENSOR USING SAME and issued to A. Laflaquiere, M. Belleville, P. Castelein, and P. Pantigny on February 1, 2005. Three of the four inventors are listed as residing in France and the fourth in Scotland. The assignee is the Commissariat a L'Energie Atomique in Paris – that is, a French government agency which deals with nuclear power.

Laflaquiere lists a PCT filing date of June 12, 2001 and seems to be a U.S. version of a French patent application filed on June 13, 2000. This is supported by the inventor residence and assignee information, as well as by unusual language which appears in the issued U.S. patent. For instance, the term "digital elementary point (PEL)" on Column 1, line 13 is consistent with a French term "pointe elementaire logicale", probably the equivalent of "pixel" in standard English technical terminology. As another example, "temps" (French for "time") appears on the x-axis of Fig. 6.

- **Laflaquiere has no valid claims**

Laflaquiere has 4 claims. Laflaquiere claim **1** is an independent claim, with each of claims **2**, **3**, and **4** being dependent claims. The text of Laflaquiere claim **4** is identical to the text of Laflaquiere claim **3**, so in fact Laflaquiere has 1 independent claim and 2 dependent claims, for a total of 3 claims.

The language of Laflaquiere claim **1** immediately rules out any valid claims.

Laflaquiere claim **1** begins on Column 8, line 66 by reciting a "device for converting an analogue signal representing charges resulting from the photo-detection of electromagnetic radiation impinging on an array of photo-detectors, into a digital signal". It is not clear what the "analogue signal" is or what the "digital signal" is, in particular because in an imaging array there are usually multiple analog signals generated

substantially at the same time, which are converted into multiple digital signals serially, in parallel, or in some mixed serial-and-parallel manner.

Regardless, the "device" is then listed as comprising, per Column 9, lines 3-7:

> a number of photo-detectors connected in rows and columns through buses, the photo-detectors in one column sharing the same column bus which is connected to an output stage through a row bus and; between each photo-detector and the column bus, further comprising:

The last phrase is important – between each photo-detector and the column bus, further comprising – and here is what is listed as being between, according to Column 9, lines 8-17 and Column 10, lines 1-8, with blank lines between the elements added for clarity:

> an integrator to integrate the charges arriving from the photo-detector;
>
> means for resetting the integrator;
>
> a comparator to compare the voltage Vp from the integrator with an internally predefined threshold voltage VS;
>
> a processing device;
>
> a clock, the clock controlling the processing device and the processing device receiving a binary value present at the output of the comparator at each signal from the clock and storing it; and
>
> digital/digital converter controlled by the clock to convert a sequence of binary values stored in the processing device into a numerical value encoded on a number of bits smaller than the number of logical values stored in the processing device.

In other words, between each photo-detector and the column bus are an integrator, a means for resetting the integrator, a comparator AND ALSO a processing device, a clock, and a digital/digital converter. This is the only way the claim can be read.

However, in the specification and figures, ONLY the integrator, the means for resetting, and the comparator are described or depicted as between each photo-detector and the column bus. The other three elements – the processing device, the clock, and the digital/digital converter – are presented as array-external parts that are shared among multiple sensor cells attached to a common column bus. They are NOT presented in the specification and figures as between each photo-detector and the column bus.

Laflaqueire Fig. 3 is identified on Column 4, lines 32-33 as "a PEL as used in the device of the invention". However, the clock (clock 8), the processing device (binary processing circuit 9) and the digital/digital converter (digital/digital converter 19) are in fact sitting at one end of a column bus (column bus 12) and not between any photo-detector and its corresponding column bus. See also the Column 4, lines 65-67 and Column 5, lines 1-4 description of Laflaquiere Fig. 2, which according to Column 4, lines 29-31 "represents schematically a read circuit including the analog/digital conversion device that is the subject of the invention.

Laflaquiere also states on Column 7, lines 36-38:

> the invention proposes that each PEL should be associated with an N bit-processing device mounted in the circuit

albeit without discussing what "the circuit" is.

Moreover, the Laflaquiere specification states with respect to Laflaquiere Fig. 3 on Column 5, lines 18-19, that "the voltage Vs is, in this diagram, obtained from an external source 25". This conflicts with the precise language of Laflaquiere claim **1** on Column 10, lines 11-12 reciting "a comparator to compare the voltage Vp from the integrator with an internally predefined threshold voltage Vs". Laflaquiere Fig. 3 therefore does not depict the invention of Laflaquiere claim **1**, nor does Fig. 4 which has the same numbered element 25. Even for Laflaquiere Fig. 6, according to Column 4, lines 37-38

"an example of the implementation of a PEL in the device of the invention", there is no guidance on the "internally predefined threshold voltage Vs" other than the uninformative Column 8, lines 53-54 statement that "the VPOL and BIAS signals are DC polarising voltages".

Another issue with respect to the "digital/digital converter" description is the meaning of the Column 10, lines 6-7 text "the number of logical values stored in the processing device". It is not clear – and is never discussed in the specification – whether the number of logical values is one if there are only binary low values or only binary high values stored and is two otherwise, or whether the number of logical values is the same as the length of the "sequence of binary values stored in the processing device" cited on Column 10, line 4.

Altogether, the result is that for multiple reasons, Laflaqueire claim **1** does not describe an invention depicted or described in the rest of the Laflaquiere patent. The claim is indefinite. Mainly, the problem is poor writing. Whomever drafted the claim neglected to properly define the scope of material included under "further comprising" so that it would conform to the discussions of the specification and figures.

Even a charitable – and improper – interpretation of Laflaquiere claim **1** as including only Column 9, lines 8-13 in the scope of the "further comprising" clause so that the elements in the claim match the structure described in the specification and figures does not render the claim definite, because the clock and processing device description on Column 9, lines 16-17 and Column 10, lines 1-2 is then indefinite because the reference "the comparator" would no longer be clear.

- **Laflaquiere claim 2 is also indefinite**

Laflaquiere claim **2** reads, according to Column 10, lines 9-11:

> Device according to claim 1, characterized in that the means for resetting include a voltage source associated with a switch.

It is a subtle difference, but by using the plural "include" rather than the singular "includes", Laflaquiere claim **2** implies that there are multiple "means for resetting in claim **1**. This implication is correct as claim **1** is written. However, claim **2** fails to state whether there are multiple voltage sources, multiple switches, or both. As claim **2** is written, the implication is that there are one "voltage source" and one "switch" associated with (e.g. for) ALL of "the means of resetting" – a situation which is not shown or suggested in Laflaquiere's figures or specification.

Laflaquiere claim **2** is therefore indefinite on its own merits and because its parent claim **1** is indefinite.

- **Finally, Laflaquiere claim 3 is also indefinite**

Laflaquiere claim **3** suffers from a similar problem to that of Laflaquiere claim **2**. Laflaquiere claim **3** reads, per Column 10, lines 12-13:

> Device according to claim 1, characterized in that the integrator is a capacitor.

This implies the existence of only one integrator, which is a capacitor. However, parent claim **1** clearly implied multiple integrators, one "between each photo-detector and the column bus". Laflaquiere claim **3** fails to indicate to which integrator "the integrator" refers, and so is indefinite.

- **Conclusions about Laflaquiere claims**

Applicant does not base assertions of Laflaquiere not anticipating the present invention solely on Laflaquiere's lack of valid claims. The point of discussing the problems of Laflaquiere's claims is to highlight that as prior art, Laflaquiere's language is unreliable, an issue that will be revisited shortly.

- **Laflaquiere's figures are unreliable**

Laflaquiere's figures are vague, confusing, and unreliable, and in one case completely wrong in some very basic aspects.

- **Laflaquiere Figs. 3 and 4 specify an externally-set threshold voltage**

As mentioned above, the discussion of Laflaquiere Fig. 3 cites on Column 5, lines 18-19, that "the voltage Vs is, in this diagram, obtained from an external source 25". Laflaquiere Fig. 4 has an identically-numbered node 25 that is never elsewhere in the specification mentioned or discussed. Presumably, it is the same as that of Fig. 3.

Comparator 26 in Laflaquiere Figs. 3 and 4 is a two-input comparator comparing an applied voltage Vp to an applied voltage Vs, the latter declared to be an externally-generated voltage. To one skilled in the art, it's clear what to do. One generates a reference voltage to be the threshold voltage, and applies it to node 25 for one input of a given sensor cell's comparator. However, the Laflaquiere claims clearly specify on Column 9, lines 13-14 an "internally pre-defined threshold voltage Vs", so Laflaquiere Figs. 3 and 4 with element 25 as defined by Column 5, lines 18-19 do not describe Laflaquiere's claimed invention.

- **Laflaquiere Fig. 5 is incorrect**

Laflaquiere Fig. 5 purports to show operation of the proposed Laflaquiere invention as embodied most specifically by Laflaquiere Fig. 6. With reference to the circuits of Laflaquiere Fig. 6 and the specification, Laflaquiere Fig. 5 includes some very basic errors.

In Laflaquiere Fig. 5, there are two voltage plots shown. The y-axis of the figure is labeled "tension" (French for "voltage") and the x-axis is labeled "temps" (French for "time). One of the voltage plots begins at a y value of Vr and after a time of t1 starts to decrease in a linear ramp until it reaches the x-axis. Simultaneously, the other voltage plot starts at an unlabeled y-value above the x-axis, and undergoes a step transition up to another unlabeled y-value which is clearly depicted as being above the y-value Vr.

In Fig. 5, the first plot is labeled "Vp", and is identified in the accompanying discussion of Column 6 as the voltage of the integrator applied to the comparator input. The second plot is labeled with a script "s", which is identified as the voltage of the comparator output.

- One or both of the "s" plot high and low levels are incorrect

A first error in Fig. 5 is that the "s" plot maximum level is incorrect. Laflaquiere Fig. 6 shows quite clearly that the reset voltage Vr is the same as the positive power supply voltage. Transistor 33 in Fig. 6 CANNOT pull the "s" node to a value above Vr. The highest it can pull the node is Vr itself.

Moreover, the low voltage for the "s" plot is also of dubious merit. It is above the minimum level reached by the Vp plot, which in principal is the voltage of the negative power supply (e.g. ground). The figure implies either that the comparator output logical low level is well above the ground voltage, or else that the integrator voltage can drop well below the ground voltage, neither of which makes sense in the context of Laflaquiere Fig. 6.

- The transition of the "s" plot from low to high is incorrect

The comparator 26 circuit symbols in Laflaquiere Figs. 3 and 4 do not include the standard "+" and "-" signs on the input terminals, so in fact there's no way of telling from the figure alone whether the comparator output should be high when Vp is greater than the supplied Vs or high when the Vp is less than the supplied Vs. This ambiguity would be acceptable given a consistent presentation elsewhere.

In the specification of Laflaquiere there are several references to comparator function. Column 3, line 60 references "when the threshold value is exceeded". Column 4, lines 1-2 refer to "the instant of exceeding the threshold value". Column 6, lines 65-67 and Column 6, lines 1-2, discussing Fig. 4, read:

> when the read voltage Vlec at the terminals of the integrator 22 exceeds the threshold value, that is as soon as the voltage Vlec becomes greater than or equal to the threshold voltage Vs, the output of the comparator 26 changes.

Column 6, lines 31-34, discussing Fig. 5, read:

> It can therefore be seen from Fig. 5 that before exceeding the threshold value Vs and consequently the resultant toggling fo the output s of the comparator 26, each scan, that is, each bit value obtained at the output s, sends a logical 0 to the column bus 12. When the threshold Vs is reached and exceeded, the logical state of the output s changes; the scans therefore send the binary value 1 to the column bus 12.

Fig. 5 does show a procession of binary 0 values followed by a procession of binary 1 values as comparator outputs, but the transition comes when the Vp plot drops below the nominal threshold voltage Vs, NOT when the Vp plot exceeds the threshold value Vs.

The inconsistency of what Laflaquiere describes and what Laflaquiere shows aside, with reference to Fig. 6, Vp of Fig. 5 is the voltage at node 35 – the lone signal input to comparator 26 – and "s" of Fig. 5 is the voltage at the node labeled "s", which is the output of comparator 26.

Consider what happens when Vp is high in Fig. 6 – that is, near the power supply voltage Vr. The gate voltage of transistor 31 is high, which means that transistor 31 is strongly on and attempting to pull the node its drain shares with that of transistor 32 and the gates of transistors 33 and 34 down toward ground. While Laflaquiere made no mention of the details of transistors 31 and 32, if the shared node is to approach ground, transistor 31 when on must be able to overpower transistor 32, which always has the same gate voltage and is thus always on (or always off – Laflaquiere never states one way or the other). In any case, when the shared node is pulled low, the gate voltages of transistors 33 and 34 are low. Transistor 34 shuts off, and transistor 33 pulls the node "s" high.

Similarly, when Vp at node 35 is low – that is to say, near ground – transistor 31 shuts off, and transistor 32, if it's on, pulls the voltage of the shared node up towards Vr. When the voltage at the gates of transistors 33 and 35 is high, transistor 33 shuts off and transistor 34 pulls the "s" node low.

In other words, when Vp is high, the voltage at node "s" is high, and when Vp is low, the voltage at node "s" is low. If Vp switches from low to high, the voltage at node "s" also switches from low to high. However, Vp does not switch from low to high. It switches from high to low – as depicted in Fig. 5. On the other hand, Fig. 5 shows the voltage at node "s" starting low when Vp is high and transitioning to high when Vp becomes lower than Vs.

- **Conclusions about Laflaquiere's figures**

As discussed just above, the figures of Laflaquiere are inconsistent with the written material in Laflaquiere's specification and also with the material in Laflaquiere's claims. Laflaquiere Figs. 1-4 are very broad, with black-box elements whose purposes and operation are never clearly explained in narrow, definite terms. Laflaquiere Fig. 5 contains fundamental errors which are in conflict with the basic building blocks of Laflaquiere Fig. 6.

The next section of this Amendment C discusses Laflaquiere's specification and is followed by further analysis of Laflaquiere Fig. 6.

Laflaquiere's specification is unreliable

Thus far, Applicant has presented compelling evidence that Laflaquiere's claims are indefinite and that Laflaquiere's figures are unreliable. Laflaquiere's specification also has problems – numerous problems – that make it unreliable as well, notably:

- There are multiple, conflicting definitions of some terms.
- Other terms are never defined or explained.
- The names associated with numbered figure elements change.
- The Columns 4-5 explanation of switch 13 in Fig. 2 is incorrect.
- The Column 7 explanation of coding is unclear and in conflict with the claims.
- The Column 8 explanation of the underlying principles of the invention is incorrect.

- **There are multiple, conflicting definitions of some terms**

As a first issue, Laflaquiere does not have a consistent definition of "sensor".

- A first definition of "sensor"

Laflaquiere states in Column 1, lines 21-23 that:

> In the field of photo-detection, sensors are classically used to convert the photo-signals delivered by basic photo-detectors into electrical signals.

While it may be the case that some sensing systems have devices which produce photons (a.k.a. "photo-signals"), in CMOS imaging arrays, the photo-detectors themselves produce electrical signals in response to incident radiation. With reference to Laflaquiere Fig. 6, photo-detector 20 produces a voltage change in response to incident radiation interacting with the semiconductor lattice of the diode junction. The voltage change is an electrical signal, not a photo-signal.

However, Laflaquiere states in Column 1, lines 39-42 that

> Each PEL comprises a photo-detector that performs a first conversion of the photo-signal into a quantity that can be processed by the read circuit, that is a current, a voltage, or a charge.

Together, these two statements at the start of Laflaquiere imply an equivalency between "photodetector" and "sensor" – that the photo-detectors are the sensors. This is in accordance with Applicant's intent and discussion in the original Application, as clarified by the present Amendment C.

- A second definition of "sensor"

Laflaquiere continues in Column 1, lines 37-39, stating "Whatever technique is used to produce them, the sensors consist of an array of elementary points called 'PELs' connected in rows and columns." In patent writing, "consist" has a very narrow limiting interpretation. Laflaquiere is either suggesting that each sensor is an array of elementary points...connected in rows and columns or that the "sensors" altogether are an array of elementary points...connected in rows and columns.

It is certainly possible to make a photo-detection system with only one sensor, and it is possible to make a sensor array which is not "connected in rows and columns", both of which possibilities Laflaquiere precludes on the cited lines.

- A third definition of "sensor"

Referring to Laflaquiere Fig. 1, Laflaquiere Column 1, line 67 and Column 2, lines 1-5 read:

> All the signals supplied by the various column buses 2 are then injected into an output stage 7. Thus the outputs of the column buses 2 share in turn the row bus 6, itself connected to the input of the output stage. The output stage passes the information it has received to the output of the sensor.

With this statement, Laflaquiere suggests that all of the cells in an imaging array sharing buses by column and then a single row bus to an output stage 7 block, plus the buses and the output stage 7 block themselves, amount to a sensor.

Column 2, lines 6-10 continue with the statement:

> The sensors are in general of the analog type. In this case, the principle of passing the information to the output of the sensor relies on two-stage multiplexing, that is multiplexing the PELs onto the column bus, then multiplexing the column buses onto the row bus.

This suggests once more that sensor encompasses an imaging array and supporting circuitry, and is further reinforced by Laflaquiere's Column 7, line 49 recitation of "sensor output 17" with reference apparently only to Laflaquiere Fig. 2.

- A fourth definition of "sensor"

Laflaquiere creates more confusion in Column 2, lines 29-34, stating:

> In order to avoid these various problems, digital sensors have been produced. Digital sensors offer the advantage of providing an output signal from the sensor that is already digitised and therefore requires only a simple digital interface.

In Column 2, lines 39-51, Laflaquiere refers to material in a prior art conference paper as – lines 45-47 – "a digital sensor in which the analog/digital conversion is done at the output stage. In this sensor, an analog/digital converter is inserted in the output of the read circuit". The paper apparently proposes purely serial analog-to-digital conversion of analog array outputs using one high-speed A/D converter.

Then, in Column 2, lines 52-64, Laflaquiere references material in another prior art conference paper, citing on lines 55-56 "a sensor in which an analog/digital converter is placed at the end of a column". This second paper apparently proposes parallel A/D converters operating serially on the analog array outputs from single columns. However, all of a sudden the imaging array system is a sensor and not a digital sensor.

In Column 3, lines 1-3, Laflaquiere again reverses course, referring to "the output stage of the sensor" for the first prior art conference paper.

- **Other terms are never defined or explained clearly**

In Fig. 3, Laflaquiere includes a black-box element labeled 21. In Column 5, lines 12 and 13-14, this element is identified as "impedance matching device 21", without any further discussion of structure or function.

In Fig. 5, Laflaquiere identifies "t1" and "t2" on the "temps" axis. The "t1" label apparently identifies a segment of time from the y-axis as indicated by the double-headed arrow. However, in the specification, "t1" is only mentioned on Column 6, line 10 as "the instant t1 [when] the switch is closed" – without identifying whether the switch is element 23 or element 13, both of which are switches. In the specification, "t2" is not discussed at all.

Moreover, "t_lec" is identified as "the read time" on Column 6, line 45, referring to Figs. 3 and 4, but Laflaquiere fails to explain how "t_lec" is related to an embodiment of the invention which doesn't have a constant current source "I_int" (e.g. Fig. 4) or an "impedance matching device 21" providing a constant current "I_int" (e.g. Fig. 3). For instance, in Fig. 6, while the photo-induced voltage drop across the terminals of photo-detector 20 is linear with light intensity, transistor 30 is in pinch-off when the voltage at node 35 is pulled all the way to Vr, regardless of V_pol and so "I_int" is not linearly proportional to the integrated incident energy.

Again with reference to Fig. 6, there is little or no discussion of the levels of VPOL, HRAZ, or BIAS. Column 8 lines 43-46 state:

> The signal VPOL corresponds to the polarisation voltage of the coupling transistor 30 and HRAZ to the reset clock signal; HRAZ is common for all the PELs in the array.

Column 8, lines 53-54 state:

The VPOL and BIAS signals are DC polarisation voltages

So the only guidance on VPOL, HRAZ, and BIAS are that VPOL and BIAS are constant, and that HRAZ, a "reset clock signal" is shared across the entire array. "Polarisation voltage" fails to impart any significant information – along the lines of saying VPOL and BIAS are "gate voltages", which is technically correct but uninformative.

The next paragraph on Column 8, lines 57-64 continues, stating:

> According to a variant of the invention, it is possible to provide a dedicated HRAZ signal for each row. In effect, the HRAZ clock signal of the integration capacitors 22 is the same for all the PELs in the array. Therefore the integration starts at the same instant for all the PELs. Now it is of interest that only PELs in the same row are scanned synchronously. For this it is sufficient tha teach row of PELs has its own reset signal.

So Laflaquiere is defining HRAZ alternately as shared by the whole array, unique to a given row of the array, and as a "clock signal of the integration capacitors". This is further obfuscated by the recitation of the clock and processing device function in Laflaquiere claim **1** on Column 9, lines 16-17 and Column 10 lines.

- **The names associated with numbered figure elements change**

The purpose of identifying elements in a figure with numbers is to be able to clearly identify substantially identical parts within a figure or across multiple figures. When discussing an invention in a specification, elements of the figures are referred to by a number and a corresponding descriptor.

In Laflaquiere, the names associated with some numbered figure elements change.

Column 5, line 11 makes first reference to "an integrator 22", which in the next line is further clarified by the statement that "the integrator 22 may be a capacitor". On Column 6, line 52 it is again "capacitor 22". However, Column 8, lines 3-4 refer to "the capacitor

22", before again referring to "integrator 22" on line 15, and finally referring to "integration capacitors 22" on line 59.

Column 5, line 12 recites "an impedance matching device 21". However, the only other mention of this element appears in Column 7, line 64 as "switches 13 and 21".

Referring to Laflaquiere Fig. 3, Column 5, lines 53-56 recite "a resetting device 23 and 24. The resetting devices consist of a voltage source 24 supplying a constant voltage Vr through a switch 23". However, discussion of Fig. 6 on Column 8, lines 42-43 state that "the transistor 24 resets the node 35 to the voltage Vr." In Figs. 3 and 4, it seems that element 24 is a voltage source applied to one end of element 23, a switch, while in Fig. 6 element 24 is a pass transistor which is the switch itself.

Laflaquiere uses the term "converter 19" on Column 7, line 15, the term "digital converter 19" on Column 7, line 50, and "digital/digital converter 19" on Column 5, line 42.

Laflaquiere uses the term "binary processing circuit 9" on Column 5, line 39, but the term "processing device 9" on Column 5, line 42.

Laflaquiere uses the term "digital processing device 14" on Column 5, lines 2-3, 5, and 7, but the term "processing device 14" on Column 7, lines 35-36.

- **The Columns 4-5 explanation of switch 13 in Fig. 2 is incorrect.**

On Column 4, lines 66-67 and Column 5, line 1, Laflaquiere states with respect to Fig. 2:

> Each PEL 10 is thus connected to a bus 12 by means of a switch 13 that multiplexes the data supplied by the various PELs.

There is clearly not "a switch 13 that multiplexes the data supplied by various PELs" onto the column bus. Each individual switch 13 connects an individual PEL 10 output to an individual column bus 12, and can be on or off. Together the switch 13 elements multiplex PEL outputs onto the column bus, but they do not multiplex individually.

- **The Column 7 explanation of coding is unclear and in conflict with the claims.**

In Column 7, lines 12-53, Laflaquiere attempts to describe a scheme for mapping sequences of stored comparator outputs to shorter sequences.

- The coding proposed is in conflict with the claims

Column 7, lines 30-32 read:

> In general, in order to encode the string of bits produced by scanning during a frame of N bits, there must be 2^N – 1 scans.

Column 7, lines 34-35 read:

> This encoding on 8 bits of the 2^N – 1 binary values obtained from the 2^N-1 scans, is produced by the processing device 14 for each PEL in the array.

Column 9, line 17 and Column 10, lines 1-7 – namely Laflaquiere claim **1** – recites:

> the processing device receiving a binary value present at the output of the comparator at each signal from the clock and storing it; and
>
> digital/digital converter controlled by the clock to convert a sequence of binary values stored in the processing device into a numerical value encoded on a number of bits smaller than the number of logical values stored in the processing device.

In other words, Laflaquiere claim **1** recites the "processing device" as "receiving...and storing", while the "digital/digital converter" does the encoding, while the specification in Column 7, lines 34-35 has "processing device 14" doing the encoding, but on Column 7, line 16 has "converter 19" doing the encoding and on Column 7, line 50 has "the digital converter 19" doing the encoding.

- The explanation of coding is unclear

Referring to Laflaquiere Fig.2, there are multiple PEL 10 blocks connected to a given column bus 12 each by a switch 13. All of the PEL 10 blocks on the column share a digital processing device 14, in Column 7 referred to simply as a "processing device 14".

For illustration purposes, let there be 1000 PEL 10 blocks on a given column bus 12, with "encoding on 12 bits" per Column 7, line 32. Then the "processing device 14" for the given column bus 12 receives and stores 1000 x 4095 bits = 4,095,000 bits during one frame. The "sequence" in which the bits are received depends on the order in which the 1000 PEL 10 blocks are scanned. Regardless, Laflaquiere fails to make clear what the "sequence" is other than stating on Column 7, lines 4-5 that "the data flowing in the column bus 12 corresponds to a string of bits". Laflaquiere does not specify whether or not the "string of bits" corresponds only to a time-ordered sequence of bits received via one switch 13 from a single PEL 10.

Given that the "processing device 14" can store around 4 million bits in the example above, there are a wide variety of coding schemes which can convert "a sequence of binary values stored in the processing device into a numerical value encoded on a number of bits smaller than the number of logical values stored in the processing device". For instance, one could take a string of 4095 bits provided by the scan of a given PEL 10 during a frame, repeat the string 1000 times, and drop the last bit. The new string would have 4,095,000 – 1 = 4,094,999 bits – many more than the original string, but meeting the requirements of the claims.

The description on Column 7, lines 34-49 seems to imply that – using the example again – instead of recording 4095 bit values for a given PEL 10 during a single frame, the PEL 10 is associated with a log_2 (4095 + 1) = 12 bit memory, which at every scan is read, the result getting either a 0 or a 1 added to it, and the sum then being re-written. However, this would be in conflict with the Column 10, lines 3-7 description of the digital/digital converter:

> digital/digital converter controlled by the clock to convert a sequence of binary values stored in the processing device into a numerical value encoded on a

number of bits smaller than the number of logical values stored in the processing device

The claim specifies conversion of a sequence stored in the processing device, not addition of a received binary PEL output to a running sum. Moreover, if there were a running sum of – using the example – 12 bits of length read, added to, and re-written at every scan the resulting numerical value would be encoded on 12 bits, not on a number of bits less than 12 bits.

Further, Column 7, lines 50-53 state:

> It can therefore be seen that the digital converter 19 converts the sequence of M binary values stored in the processing device into a digital value encoded on a number of bits which is smaller than M.

This reinforces the idea – inefficient though it may be – of storing all the received scan results for a given PEL, then encoding to a smaller number of bits than the number of scans, the prior reference to M being on Column 3, line 51 as the number of scans per frame for a given PEL.

- **The Column 8 explanation of the underlying principles of the invention is incorrect.**

Laflaquiere Column 8 ostensibly contains some analytical justification of the invention, but in fact is rife with basic errors. Overall, a few errors here or there in a piece of prior art can be explained away as typos, but the fact is that errors in Laflaquiere are pervasive, which makes it difficult to determine exactly what Laflaquiere suggests as prior art.

- Column 8 paragraph 1 flaws

Laflaquiere Column 8, lines 1-9 read:

> In addition, this digital sensor has the advantage of being able to be easily modified, that is converted from application to another since only the values of the capacitor 22 and the voltages Vr and Vs must be redefined to ensure the same transfer function, in accordance with the equation given above. The sensor is therefore compatible with so-called "low voltage" technology as well as with SOI (Silicone on Insulator) technology since few electrical devices process analog quantities.

The "equation given above" cited by Laflaquiere is apparently that of Column 6, lines 48-49, namely t_lec = C_lec x (Vr – Vs) / I_int.

Note that the entire invention is referred to as "this digital sensor" in Column 8, line 1 – another switch in the scope and definition of "sensor". Also, the "equation given above" implies a positive t_lec, but in conjunction with Figs. 3, 4, and 5 we see that I_int is depicted as flowing into the integrator when it is properly flowing out of the integrator. This makes t_lec as defined by the authors a negative time. Moreover it is not at all clear what the authors mean by "same transfer function". It is certain that changing Vs by modifying the relative sizes of transistors 32 and 31 in Fig. 6 or by changing the value of the BIAS voltage applied to the gate of transistor 32 will NOT result in a "same transfer function", because the voltage at the shared drain node of the two transistors is a non-linear function. This will be discussed further in the section on Office Action C interpretation of transistor 31 as merely "coupling" the voltage at node 35 to the gates of transistors 33 and 34.

The sentence at the end of Column 8, paragraph 1 also has several problems. For one thing, the circuit of Fig. 6 in fact is NOT all that compatible with "low voltage" technology. Transistor 30, whose operation is never fully explained other than that V_pol is a "DC polarising voltage" (Column 8, lines 53-54), cannot pass a strong logic 1 signal. When the voltage at node 35 is pulled up to Vr, the voltage at the cathode of photo-detector 20 can reach at most one threshold drop less than Vr. Further, transistor 32 is always on, so the circuit dissipates quiescent power, and if the circuit is replicated, say, 10 million times, will dissipate a lot of quiescent power. "Silicone on Insulator" is not a semiconductor technology. Probably the authors meant "Silicon on Insulator" and the use of "silicone" is a typo. With respect to the assertion that "few electrical devices

process analog quantities" – presumably referring to the digital PEL output rather than an analog output, the part count is quite high – a photo-detector, a pass transistor, a reset transistor, a capacitor-configured transistor, transistor 32, transistor 31, and circuits to provide BIAS – relative to the Applicant's invention and even relative to prior art such as the three-transistor CMOS APS cell.

- Column 8 paragraphs 2 and 3 flaws

Column 8, lines 10-22 read as follows:

> As described above, the principle of reading the PEL 10 relies on exceeding the threshold of comparison Vs. It is the instant t_lec of exceeding this threshold that permits encoding of the photonic input current in time. Therefore, whatever the current I_int, the number of charges integrated in the integrator 22 is the same.
>
> If we call the maximum total charge that can be stored in the integrator Q_max, then Q_max = q N_max = C_lec (Vr – Vs) = I_int t_lec Where q is the charge of one electron (q=1.6e-19C) and N_max is the maximum number of charges corresponding to Q_max.

With respect to the first of these two paragraphs, the issue of using the term "exceeding" when in fact the integrating capacitor voltage starts high and then drops has been discussed.

The statement that "whatever the current I_int, the number of charges integrated in the integrator 22 is the same" is misleading and incorrect. The number of charges integrated in the integrator 22 depends on the amount of light incident on photo-detector 20 (referring to Fig. 6). In weak light, voltage change corresponding to the integrated charge may never reach drop the voltage at node 35 to Vs. In stronger light, this voltage may reach Vs – but it may continue to decrease thereafter.

Therefore, the discussion of Q_max is incorrect. The "maximum total charge that can be stored in the integrator" is in fact a function of the size and composition of the integrator, and is largely limited by dielectric breakdown. The maximum charge that actually is

stored in the capacitor in Fig. 6 is likely to be much less than this, but at any rate is equal to C_lec Vr. The charge is stored there by the process of resetting node 35 and removed as photo-generated electron-hole pairs in the photo-detector 20 are swept to the photo-detector's charged plates.

- Column 8, paragraphs 5-6 flaws

In Column 8, lines 23-36, Laflaquiere define "the effective value of noise associated with a photodiode integrating N charges in a capacitor", but for "detectors" which are "of the quantum type". In Column 1, lines 27-33, Laflaquiere specifically discussed "photodiodes or photo-arrays of CMOS sensors" and "so-called 'quantum' photo-detectors" as different devices.

With respect to the "signal/noise" ratio, it's true that the photon interaction in the photo-detector is a random process, that interaction IS the signal. The measurement of the "signal" is not "the maximum number of charges corresponding to Q_max", it is the time required from the start of integration for the integrating capacitor to trigger switching of the output of comparator 26. Even with no other sources of noise and an ideal zero-variation inter-photon-arrival time, there is a fundamental measurement limit which depends on the rate at which the comparator output can be checked, and in a large array the checking is necessarily relatively infrequent. But of course there is thermal noise in all of the circuit components of Fig. 6.

It simply isn't clear what Laflaquiere's definition of S/N ratio means or even why it was included in Laflaquiere's specification.

Discussion of Office Action C rejections under 35 U.S.C. 102(e)

On pages 3-11, Office Action C rejected Application claims **2-5** and **7-20** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. The rejected claims include independent claim **2** and its dependent claims **3-5**, independent claim **7** and its dependent claim **8**, independent claim **9** and its dependent claim **10**, independent claims **11, 12,** and **13**, independent claim **14** and its dependent claims **15-18**, and independent claim **19** and its dependent claim **20**. Also, claim **6** was objected to as dependent on a 102(e)-rejected claim but allowed pending revision as an independent claim.

Each claim rejection under 35 U.S.C. 102(e) cites Figure 6 of Laflaquiere and identifies elements and groups of elements in Fig. 6 as analogous to elements in a given claim. However, for a claim to be anticipated by prior art, ALL of the limitations of the claim must be shown or suggested by the prior art. Applicant respectfully submits that it is NOT the case that ALL of the limitations of the rejected claims are shown in Laflaquiere Fig. 6 or shown or suggested elsewhere in Laflaquiere. This is because Office Action C misinterprets the nature of transistors 31 and 32 of Laflaquiere Fig. 6, attributing to them a simple "coupling" function between node 35 and the gates of transistors 33 and 34. In fact, transistors 31 and 32 implement monotonic, non-linear, affine transformation of the signal at node 35, so that the signal at the gates of transistors 33 and 34 is NOT the signal at node 35.

- **Discussion of transistors 31 and 32**

Office Action C relies on the assumption that transistors 31 and 32 "couple" the signal at node 35 to the gates of transistors 33 and 34. However, it does not actually discuss or analyze these transistors. Further, Laflaquiere never discusses any details of transistors 31 and 32. The two transistors and their connections are shown in Fig. 6, but Laflaquiere makes no mention whatsoever of absolute or relative transistor size, valid levels of the BIAS signal applied to the gate of transistor 32, or generation of the BIAS signal.

Office Action C states on page 4 line 8 that the signal at "input node 35 is coupled to [the] gates of 33 and 34 via 31 and 32". The implication is that the circuit defined by

transistors 33 and 34 is little more than a switch, a notion which is very much not the case.

A careful consideration of transistors 31 and 32 reveals that they form a circuit similar to a pseudo-NMOS inverter. The enclosed material from the introductory textbook CMOS VLSI Design by Weste and Harris depicts a pseudo-NMOS inverter, particularly in Fig. 2.30 of page 101. As discussed earlier with respect to Laflaquiere Fig. 5, transistor 31 of Laflaquiere Fig. 6 is a pull-down transistor. When the voltage at its gate is high, it turns on and attempts to pull the voltage at the node it shares with transistor 32 down toward ground. When the voltage at its gate is low, it turns off, and leaves transistor 32 to set the voltage at the shared node. Transistor 32, in turn, is a pull-up transistor. It has a fixed voltage BIAS at its gate. Unless this voltage is too close to Vr, it is always on, and always trying to pull the voltage of the node it shares with transistor 31 up to Vr.

With reference to Weste and Harris Fig. 2.30c, if the input to transistor 31 of Laflaquiere were a small signal on top of a proper DC gate bias voltage, the output at the shared drain node of the transistor would be a linearly amplified version of the input small signal riding on a DC output voltage. The AC small-signal gain would be determined by the slope of the V_in-V_out curve at the bias point. In such a situation, the AC output voltage would be a scaled version of the small-signal AC input voltage. One might then treat transistors 31 and 32 as "coupling" the input to the output, albeit with some non-zero gain G. A more accurate description would be that the transistors "amplify" the small-signal input.

However, as is clear, notably from Laflaquiere Fig. 5, the voltage at node 35 is NOT a small signal. It can sweep potentially from Vr all the way down to ground. This means that the output voltage at the shared drain node of transistors 31 and 32 potentially sweeps from close to ground all the way up to Vr. Transistor 32 is either always on or always off, depending on the value of BIAS. Assuming that it's on, the shared drain node is never pulled all the way down to ground.

Transistors 31 and 32 have a DC transfer function similar to that of Weste and Harris Fig. 2.30c. This input-output relation is clearly non-linear and monotonic. Mathematically, there is in theory exactly one point on the transfer function curve at

which the input equals the output, but at every other point the two are not the same. Moreover, it isn't even the case that the output signal is the input signal multiplied by some constant gain G. It is therefore unreasonable to claim that transistors 31 and 32 "couple" the signal from node 35 to the node shared by transistors 31 and 32. The signal at the gates of transistors 33 and 34 is a function of Vp, but is certainly not Vp itself. It is NOT the same as the signal at node 35.

- Transistors 31 and 32 and prior art teach away from using the circuit of Fig. 6 and internal BIAS generation in the context of an array

Laflaquiere does not provide any details of the value or generation of BIAS, other than stating that it can be generated externally to the pixel or internally. BIAS might be "generated" internally by tying the gate of transistor 32 to Vr, in which case transistor 32 is always strongly on. Alternatively, a non-Vr BIAS can be generated with a ratioed pair of complementary transistors, with a resistive bridge, and so on. Weste and Harris discuss using one pair of ratioed transistors to generate gate biasing signals for multiple pseudo-NMOS inverter circuits, which is advantageous because even if the generating transistor dimensions are inaccurate, the gate bias voltages are all the same.

From a perspective of imaging system design, the presence of transistor 31, transistor 32, and internally-generated BIAS is bad for two reasons. Suppose that there are 5 million pixels in a system according to Laflaquiere, a pixel count which is quite common in currently-available digital imaging systems. This means 5 million transistors 31, 5 million transistors 32, and at least 10 million ratioed transistors for internal generation of BIAS. Or, worse, there could be at least 10 million resistors for internal generation of BIAS. That's a lot of circuit elements taking up a lot of chip space, and to boot it's likely that they won't be well-matched.

The real problem, though, is that the BIAS generation circuits and the transistor-32-transistor-31 pairs will all draw quiescent current. When, referring to Fig. 5, Vp is up high near Vr, both transistor 32 and transistor 31 will be going full bore, and a massive amount of current will be passing through them. Even if "massive" is a really small current, with 10 million similar circuits operating simultaneously, there is a huge amount of static power dissipation.

Therefore, the prior art teaches away from internal generation of BIAS, on the basis of matching, chip space, and power consumption, and also teach away from using Laflaquiere's Fig. 6 circuitry in CMOS image sensor arrays on the basis of chip space and power consumption requirements.

- **Discussion of 102(e) rejection of claim 2**

On pages 3-4, Office Action C discusses reasons for rejecting Application claim **2** as anticipated by Laflaquiere. Particularly, Office Action C identifies a first sensor comprising "photo-detector 20, switch 30, integrator 22, [and] reset device 24" and having as a first sensor output the signal appearing at node 35.

With respect to this first sensor, in Laflaquiere's specification itself, element 30 is only ever identified as "a transistor 30" (Column 8, line 39) and "the coupling transistor 30" (Column 8, line 44), and never as a switch. Further, Laflaquiere identifies the gate voltage VPOL of element 30 as one of two "DC polarising voltages" (Column 8, lines 53-54), which suggests that the element is not a switch. Laflaquiere's specification also refers to element 22 as "integrator 22" in multiple locations but also as "the integration capacitors 22" (Column 8, line 60). Laflaquiere's specification refers to element 24 as "transistor 24" (Column 8, line 42) but also as part of "a resetting device 23 and 24" (Column 5, line 54) particularly as "a voltage source 24 supplying a constant voltage Vr through a switch 23" (Column 5, line 55) with reference to Fig. 3.

Office Action C further identifies Laflaquiere's "comparator 26" of Fig. 6 as a threshold detector having a first analog input "coupled to node 35" and a first digital output at node beta (a script S according to Laflaquiere). This threshold detector comprises, according to Office Action C, a first transistor in the form of transistor 34 having a first gate and a second transistor in the form of transistor 33 having a second gate.

Office Action C then states the following on Page 4, lines 7-8 that Laflaquiere Fig. 6 includes:

means for applying the first analog input to the first gate and to the second gate (input node 35 is coupled to gates of 33 and 34 via 31 and 32)

The answer to the fundamental question "Do transistors 31 and 32 apply the first analog input to the first gate and to the second gate?" is an unequivocal "NO". The signal at the first analog input identified by Office Action C is the signal at node 35. This is NOT the same signal that appears on the drain of transistor 31 and which is applied to the first and second gates.

Therefore, Laflaquiere Fig. 6 does NOT show element b-iii of Application claim **2**, "means for applying said first analog input to said first gate and to said second gate". In contrast, the Application figures show and the Application specification discusses passing the sensor output directly to the first gate and the second gate of the transistors recited in claim **2**.

- **Discussion of 102(e) rejection of claims 3-5**

On pages 4-5, Office Action C rejects claims **3-5** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. These three claims are all dependent claims of claim **2**, and so have all of the limitations of claim **2**. As discussed above, Laflaquiere Fig. 6 does not have element b-iii of claim **2**, and therefore does not have all the limitations of dependent claims **3-5**.

- **Discussion of 102(e) rejection of claim 7**

On page 5, Office Action C rejects independent claim **7** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. Office Action C stated on page 5, lines 11-13, that Laflaquiere Fig. 6 shows, with underlining by Applicant:

means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32)

As discussed above, the signal applied to the gates of transistors 33 and 34 in Laflaquiere Fig. 6 is NOT the signal at node 35. However, on page 5, lines 11-13, Office

Action C clearly articulates the previously-discussed misinterpretation that transistors 31 and 32 simply couple the signal at node 35 to the gates of transistors 33 and 34.

Applicant submits that Laflaquiere Fig. 6 fails to have the cited "means for applying the first analog input to the first gate and to the second gate" because the first analog input is not applied to either gate. Laflaquiere Fig. 6 does not have the limitation b-iii of claim **7**.

- **Discussion of 102(e) rejection of claim 8**

On pages 5 and 6, Office Action C rejects dependent claim **8** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. Claim **8** is dependent on independent claim **7**, and so has all of the limitations of claim **7**. As discussed above, Laflaquiere Fig. 6 does not have element b-iii of claim **7**, and therefore does not have all the limitations of dependent claims **8**.

- **Discussion of 102(e) rejection of claim 9**

On pages 6 and 7, Office Action C rejects independent claim **9** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 7, lines 7-9, Office Action C recites the following as present in Laflaquiere Fig. 6:

> means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32)

As previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitation of claim **9** part b-iii, namely "means for applying said first analog input to said first gate and to said second gate".

Moreover, Laflaquiere clearly states that comparator 26 – which Office Action C identifies as the threshold detector – has an adjustable threshold level. This is clearly shown in Fig. 3, which according to Column 4, lines 32-33 "represents schematically a PEL as used in the device of the invention" and in Fig. 4, which according to Column 4,

lines 34 "shows an electrical diagram of the PEL in FIG. 3". Each has "an external source 25" (Column 5, line 19, underlining by Applicant).

Subsequently, on Column 5, lines 19-22, Laflaquiere states with reference to the threshold voltage Vs that:

> It can also be defined by the internal characteristics of the comparator (that is the intrinsic characteristics of the transistors forming the comparator) and then does not require the external source.

However, in Fig. 6, the threshold voltage Vs – whatever it happens to be – is clearly not defined solely by "the intrinsic characteristics of the transistors forming the comparator". Fig. 6 clearly shows that there is also a gate voltage BIAS is applied to transistor 32. However, Laflaquiere provides no further guidance on "the intrinsic characteristics of the transistors forming the comparator" and includes absolutely no discussion of valid levels of BIAS or of how to generate BIAS. If BIAS generation circuitry is shared among multiple PELs – a distinct possibility in the context of an array – then comparator 26 of Laflaquiere Fig. 6 is certainly not a single-input threshold detector.

- **Discussion of 102(e) rejection of claim 10**

On page 6, Office Action C rejects dependent claim **10** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. Claim **10** is dependent on independent claim **9**, and so has all of the limitations of claim **9**. As discussed above, Laflaquiere Fig. 6 does not have element b-iii of claim **9**, and therefore does not have all the limitations of dependent claims **10**.

- **Discussion of 102(e) rejection of claim 11**

On pages 6 and 7, Office Action C rejects independent claim **11** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 7 lines 7-9, Office Action C recites the following as present in Laflaquiere Fig. 6:

means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32)

Again as previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitation of claim **11** part b-iii, namely "means for applying said first analog input to said first gate and to said second gate".

Moreover, on page 7 line 3, Office Action C asserts that the "threshold detector", namely comparator 26, is "a single-input threshold detector". Per the previous discussion for claim **9**, Laflaquiere discusses an adjustable threshold voltage, but with specific respect to Fig. 6 fails to discuss any details of the nature of the transistors comprising comparator 26 or the value(s) and source of the gate voltage signal BIAS. The only reference is the vague passing mention of Laflaquiere Column 5, lines 20-23 which fails to mention the requirement for BIAS.

Also, as mentioned above, in an array of Fig. 6 PELs, there is a clear advantage to generating BIAS separately and sharing it among multiple sensor cells. One can advance the argument that because BIAS in Fig. 6 is completely within the dashed-line box identified by the label 26, it must be internal, but this argument falls apart on consideration of Fig. 3, which has both "an external source 25" (Column 5, line 19, underlining by Applicant) and "a resetting device 23 and 24" (Column 5, lines 53-54) or "a voltage source 24" (Column 5, line 55) depicted and labeled the same way. The analogous "voltage source" in Laflaquiere Fig. 6, notwithstanding the element 24 labeling error of Fig. 6, is clearly the positive power supply Vr, which is not generated internally in comparator 26.

While Laflaquiere recites "an internally predefined threshold voltage Vs" (Column 9, lines 12-13, underlining by Applicant) in Laflaquiere claim **1**, Laflaquiere Fig. 6 and the Laflaquiere specification are vague on the issue, with the specification especially trying to recite both external and internal threshold voltages as part of the invention.

- **Discussion of 102(e) rejection of claim 12**

On pages 7 and 8, Office Action C rejects independent claim **12** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 7 lines 18-20, Office Action C recites the following as present in Laflaquiere Fig. 6:

> means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32)

Again as previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitation of claim **12** part b-iii, namely "means for applying said first analog input to said first gate and to said second gate".

Note that the common "missing part b-iii" for many of the 102(e)-rejected claims stems from the fact that many were dependent on the original claim **1** of the Application and were re-written as independent claims in a previous amendment.

- **Discussion of 102(e) rejection of claim 13**

On pages 8 and 9, Office Action C rejects independent claim **13** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 8 lines 18-20, Office Action C recites the following as present in Laflaquiere Fig. 6:

> means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32)

Again as previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitation of claim **13** part b-iii, namely "means for applying said first analog input to said first gate and to said second gate".

Further, on page 8, lines 14-16, Office Action C recites as present in Laflaquiere:

> a first transistor (34) having a first gate, the first transistor being a minimum-size transistor (34 is minimum-sized compared to a big sized power transistor)

Also on page 8, on lines 16-18, Office Action C recites as present in Laflaquiere:

> a second transistor (33) having a second gate, the second transistor being a minimum-size transistor (33 is minimum-sized compared to a big sized power transistor)

Neither Laflaquiere Fig. 6 nor any other part of Laflaquiere shows or discusses the sizes of transistors 33 and 34. Office Action C itself casually declares "minimum-sized" being relative to "a big sized power transistor", but in fact it is quite possible to have a transistor that is not of minimum size that that is smaller than "a big sized power transistor".

A "minimum size" transistor depends on manufacturing technology, and is uniquely defined for that technology. However, in CMOS processes, the carrier mobility of holes is less than that of electrons, so the gain of pMOS transistor in a given technology is less than the gain of an nMOS transistor of identical size in the same technology. In designing a digital inverter, it is typical to increase the size of the pMOS transistor so that it and the complementary nMOS transistor with which it works have the same gain. This sets the switching level at the mid-point between the power supply values, maximizing noise margin and reducing delay due to differing rise-time and fall-time values. In compound CMOS logic gates, the transistor sizes may also be scaled to balance rise and fall times in order to minimize delay.

In other words, the prior art teaches away from having both transistors be of minimum size, and Laflaquiere teaches nothing about transistor size.

- **Discussion of 102(e) rejection of claim 14**

On page 9, Office Action C rejects independent claim **14** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 9, lines 6-7 and 9-11, Office Action C recites as present in Laflaquiere Fig. 6:

a multiplicity of threshold detectors...each having an input line connected to the gates of at least two transistors (each detector 26 has two transistors 33 and 34 whose gates are coupled to the input node 35 via 31, 32)

Again as previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. The input line of comparator 26, which Office Action C identifies as the threshold detector in Laflaquiere Fig. 6, clearly has an input line that is connected to the gate of only one transistor, which is transistor 31. In Fig. 6, the element labeled 22 is depicted as a transistor symbol with both source and drain permanently connected to ground. It is only ever referred to in the specification of Laflaquiere as "integrator 22", and the same numerical label 22 appears in Laflaquiere Fig. 5 identifying a capacitor as "capacitor 22" (e.g. Column 6, line 52 and Column 8, line 59). The clear suggestion of the symbol used for element 22 in Fig. 6 is that the capacitor can be formed in a MOS fabrication process with a self-aligned polysilicon top plate over a diffusion bottom plate with a thin oxide dielectric. Aside from being a capacitor and not a transistor, element 22 is not a part of the threshold detector as defined by Laflaquiere or as defined by Office Action C.

Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitation of claim **14** part a-i, namely "a multiplicity of threshold detectors, each having" (part a) "an input line connected to the gates of at least two transistors" (part a-ii).

- **Discussion of 102(e) rejection of claims 15-18**

On page 10, Office Action C rejected dependent claims **15-18**. Claims **15**, **16**, and **17** have independent claim **14** as their parent claim, while claim **18** has claims **17** and **14** as its parent claims.

As discussed above, Laflaquiere does not have or suggest element a-i of independent claim **14**. This element is also a limitation of dependent claims **15-18**, so Laflaquiere does not have or suggest all of the limitations of those four claims.

Further, with respect to claim **15**, the previous discussion of Laflaquiere's indeterminate explanation of BIAS and whether or not comparator 26 is a single-input comparator – presented above with regard to the 102(e) rejection of claim **11** – applies.

Further, with respect to claim **18**, the previous discussion on transistor sizing and Laflaquiere's lack of any discussion whatsoever of transistor sizing – presented above with regard to the 102(e) rejection of claim **13** – applies.

- **Discussion of 102(e) rejection of claim 19**

On pages 10-11, Office Action C rejects independent claim **19** under 35 U.S.C. 102(e) as anticipated by Laflaquiere. On page 11, lines 10-13, Office Action C recites the following as present in Laflaquiere Fig. 6:

> means for applying the first sensor output to the first gate (conductor connecting the node 35 to the gate of 33 through 31 and 32), means for applying the first sensor output to the second gate (conductor connecting the node 35 to the gate of 33 through 31 and 32)

Again as previously discussed, the signal applied to the gates of transistors 33 and 34 is NOT the signal at node 35. Applicant therefore submits that Laflaquiere Fig. 6 lacks the limitations of claim **19** parts d-iv and d-v (formerly e-iv and e-v).

Further, on page 11, lines 3-5, Office Action C recites as present in Laflaquiere Fig. 3:

> a first digital counter providing a digital elapsed time count (converter 19 in Fig. 3 performs counting 0s and 1s and provides digital values; col. 5, lines 41-44)

However, Laflaquiere Column 5, lines 41-44 read as follows:

> A digital/digital converter 19 controlled by the clock 8 receives the binary values from the processing device 9 and converts the sequence of 0s and 1s into digital values.

Laflaquiere does not clearly indicate that "digital/digital converter 19" is a first digital counter providing a first digital elapsed time count. In fact, the discussion of the operation of element 19 in Column 7 of Laflaquiere is ambiguous. Column 7, lines 38-46 imply some sort of comparator output counting. However, Column 7, lines 50-53 state the following:

> It can therefore be seen that the digital converter 19 converts the sequence of M binary values stored in the processing device into a digital value encoded on a number of bits which is smaller than M.

This implies that digital converter 19 simply takes a string of M binary values after they've been acquired and produces a shorter string at some later time, in which case it is not providing a digital elapsed time count, so that Laflaquiere lacks the limitation of Application claim **19** part c (formerly part d), "a first digital counter providing a first digital elapsed time count".

If one takes a favorable view of Laflaquiere's confusing discussion and declares, as Office Action C asserts on page 11, lines 3-5, that converter 19 of Fig. 3 is "a first digital counter providing a digital elapsed time count (converter 19 in Fig. 3 performs counting 0s and 1s and provides digital values; col. 5, lines 41-44)", then Laflaquiere further lacks the limitation of Application claim **19** part e (formerly part f), namely "means for recording a first value of said digital elapsed time count on the basis of a change in said digital indicator output signal". Office Action C asserts presence of this limitation on page 11, line 15, citing "digital values are stored in a memory, col. 7, lines 38-40", but in so doing sets up a situation where the "first digital counter providing a digital elapsed time count" and the "means for recording a first value of said digital elapsed time count on the basis of a change in said digital indicator output signal" are the same element of Laflaquiere, but separate and distinctive in Application claim **19**. On its own, the memory cited by Office Action C could amount to "means for recording a first value of said digital elapsed time count", but would not amount to "means for recording a first value of said digital elapsed time count on the basis of a change in said digital indicator output signal" without being part of the converter 19 function cited on Office Action C page 11, lines 3-5.

- **Discussion of 102(e) rejection of claim 20**

On page 11, Office Action C rejected dependent claim **20**. Claim **20** has independent claim **19** as its parent claim. As discussed above, Laflaquiere does not have or suggest elements d-iv and d-v (formerly e-iv and e-v) of independent claim **19**, and so Laflaquiere does not have or suggest all of the limitations of dependent claim **20**.

The additional missing limitations discussed above with respect to claim **19** also apply to claim **20**.

Moreover, Office Action C states on page 11, lines 17-19 that:

> the means for detecting when the first sensor output reaches the first threshold level is an inverter (comparator 26 in Fig. 6 has an inverter comprising 33 and 34)

Comparator 26 has an inverter but is not itself an inverter. Claim **20** part a recites that the "means for detecting...is an inverter". Therefore, Laflaquiere lacks the limitation of claim **20** part a.

- **Conclusions about Office Action C rejections under 35 U.S.C. 102(e)**

For each of the claims rejected by Office Action C under 35 U.S.C. 102(e) as anticipated by Laflaquiere, Applicant has demonstrated that at least one claim limitation is not shown or suggested in Laflaquiere. Where relevant, Applicant has also mentioned additional limitations of individual claims that are not shown or suggested in Laflaquiere.

The main reason why the rejected claims are not anticipated by Laflaquiere is that Office Action C misinterprets the function of transistors 31 and 32 in Laflaquiere Fig. 6 as "coupling" the signal at node 35 to the gates of transistors 33 and 34. In fact, the signal at the two gates is NOT the signal at node 35, as discussed in detail above.

Further, Applicant has clarified that in CMOS image sensor arrays, the "sensors" are "photodetectors", in keeping with the discussion of the Application's specification and

figures. This change makes clear the novelty of the present invention, particularly in light of the issue raised by Office Action C and also by analysis of Laflaquiere that "sensor" in the prior art may be a poorly-defined term with conflicting definitions of varying scope.

Applicant therefore submits that claims **2-5** and **7-20** are not anticipated by Laflaquiere, and requests withdrawal of rejection of these claims under 35 U.S.C. 102(e). Applicant submits that these claims, as well as claim **6**, are therefore in condition for allowance, and requests same.

Regarding allowable subject matter

On page 12, Office Action C objected to claim **6** as dependent on rejected claims but allowed the claim pending re-writing as an independent claim with all the limitations of rejected parent claims.

As discussed above, Applicant submits that the parent claims of objected-to claim **6** are in fact allowable, and therefore that claim **6** is also allowable without re-writing as an independent claim.

Regarding prior art made of record and not relied upon

On page 12, Office Action C cites two additional U.S. Patents as relevant to the Application, but does not otherwise comment on or discuss them. These two patents are U.S. Patent 6,940,443 and U.S. Patent 6,943,719.

- **Comments on U.S. Patent 6,940,443**

U.S. Patent 6,940,443 is entitled ANALOG TO DIGITAL CONVERTER WITH A PULSE DELAY CIRCUIT and was issued to T. Terazawa and T. Watanabe on September 6, 2005. The filing date of the patent is September 16, 2004.

The invention of Terazawa et al. is basically a voltage-to-frequency converter. The voltage is an unknown analog input to an A/D converter, and is supplied as the positive power supply voltage to a ring oscillator composed of a circularly-connected set of inverters. The unknown analog voltage would probably have to be derived from an op-amp output capable of sourcing or sinking enough current to serve as the power supply for the ring oscillator. The ring oscillator relies on inverter delay in order to function. Each inverter in the ring adds additional delay. The delay is due to inverter outputs charging and discharging capacitance of connecting wires and the gates of inverter inputs, and possibly also dedicated capacitors.

With a constant power supply voltage, the ring oscillator is basically a fixed-frequency clock source. However, Terazawa et al. modify the power supply voltage according to the unknown input. This changes the amount of charging and discharging the component inverter outputs must accomplish, which changes the inverter delays, which changes the frequency of the ring oscillator. A digital output for the A/D converter is produced by counting pulses in the ring oscillator, which is equivalent to measuring the frequency.

Terazawa's invention is ill-suited to CMOS imaging arrays. For one thing, it is purely serial. Only one A/D conversion can be accomplished per ring oscillator per full count cycle, which is 2^N counts for N-bit conversion. Moreover, after this conversion is accomplished, additional processing is necessary to obtain a uniform digital mapping,

which will be less than N bits and which requires an accurate model of the relationship between input voltage and frequency, a relationship which is nonlinear according to Terazawa Fig. 9.

Further, in a CMOS imaging array, each ring oscillator would definitely require an analog signal buffer. Photodetectors do not provide enough charge to power one inverter directly let alone a ring oscillator composed of multiple inverters. There is also the problem of array size. With a 5-million-pixel CMOS imaging array, 5 million dedicated ring oscillators plus supporting circuitry would likely be grossly impractical, which leaves the Terazawa invention as just one of many possible A/D converters in an array-external multiplexed structure – such as the by-rows-and-columns or column-dedicated-row-shared architectures of Laflaquiere Fig. 1 and the two conference papers cited in Laflaquiere.

- **Comments on U.S. Patent 6,943,719**

U.S. Patent 6,943,719 is entitled ANALOG-TO-DIGITAL CONVERTER FOR IMAGE SENSOR and was issued to Young-Hwan Yun and Dong-Hun Lee on September 13, 2005. The filing date of the patent is listed as August 21, 2003.

In the Yun et al. invention, with reference to Fig. 2, the photodetector (PD1) output is passed to an in-cell amplifying transistor (103) whose output is selectively applied to a column bus (14) by a row-select transistor (104). This passes the amplifying transistor output out of the array to an external A/D converter. The signal is passed to a summing junction (the node by VA) through a switch (SW1) and a capacitor (C1). Simultaneously, a reference ramp voltage (VRAMP) is passed to the same summing junction via another switch (SW2) and another capacitor (C2). The signal VA is thus a linear combination of the amplifying transistor output and the reference voltage ramp signal VRAMP. It drives an inverter circuit with a selective enable control (121).

In operation, as depicted in Yun et al. Fig. 5, VA is initially set to half of the positive power supply voltage, Vdd/2. Note that this is a theoretical Vdd/2 achieved by connecting the inverter circuit 121 output back to the inverter circuit 121 input. In practice, the level will depend on the transistor gains, which in turn depend on the

transistor sizes and intrinsic carrier mobility values, with different instances of the circuit (e.g. for different columns of sensor cells) having different initial reset values.

The amplifying transistor output is sampled before the photodetector output is applied to it, and after (this is correlated double-sampling CDS). The "before" sample is stored on capacitor C1 during the reset sampling period. The "after" sample is added to the summing junction during the signal sampling period, changing VA. At the same time (during the signal sampling period), the ramp signal is applied to the summing junction, but the ramp does not start rising until after the CDS is complete. When the ramp finally starts to rise, a digital counter begins to count (providing CNT). The inverter with selective enable control (121) undergoes an output transition when the input (VA) rises above Vdd/2, which causes another inverter (122) to make a latch (123) record a value of the digital count.

Yun et al. therefore implements correlated double sampling of an in-cell amplifying transistor output. It removes this sample from a charged node, and afterwards adds charge to the node at a constant rate, creating an offset voltage ramp. It then implements a form single-slope A/D conversion, comparing the offset voltage ramp to the input switching level of an inverter. Note that the typical form of single-slope A/D conversion is comparing a known voltage ramp to a held, unknown voltage, whereas Yun et al's single-slope A/D conversion compares a known voltage ramp plus an unknown offset to a held, constant voltage which may be known or unknown.

Conclusion

For all the above reasons, the Applicant submits that the specification and the claims are now in proper form, and that the claims are all patentable over the prior art. Therefore, the Applicant submits that this application is now in condition for allowance, which action is respectfully solicited.

Conditional Request for Constructive Assistance

The Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, the Applicant, an independent inventor and pro se filer, respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P SS 2173.02 and SS 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very Respectfully,

Charles D. Murphy

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Evanston, IL 60202
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Certificate of Mailing: I hereby certify that this correspondence, and attachments, if any, will be deposited with the United States Postal Service by ~~Overnight~~ FIRST CLASS Mail, postage prepaid, in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

February 23, 2006 Charles Douglas Murphy

Charles Douglas Murphy, Applicant

Source: CMOS VLSI DESIGN, 3rd ed., by N.H.E. Weste + D. Harris, Pearson Education, Inc. 2005

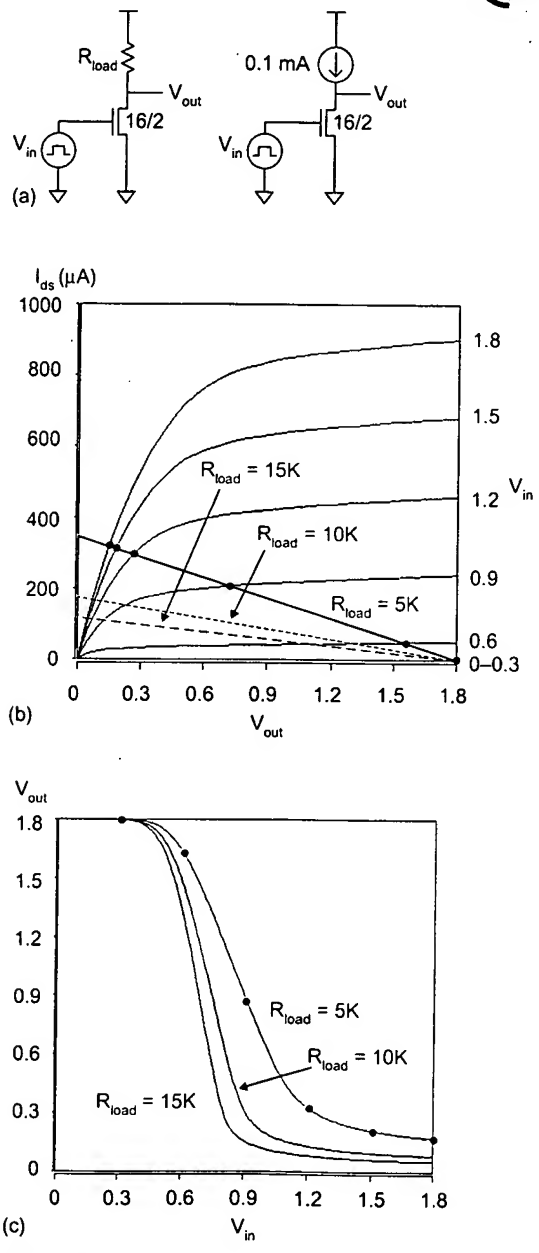

FIG 2.29 Generic nMOS inverters with resistive or constant current load

OPTIONAL

2.5.4 Ratioed Inverter Transfer Function

Apart from the complementary CMOS inverter, there are other forms of MOS inverter that can be used to build logic gates. Figure 2.29(a) shows a generic nMOS inverter that uses either a resistive load or a constant current source. For the resistor case, if we superimpose the resistor load line on the I-V characteristics of the pulldown transistor (Figure 2.29(b)), we can see that at $V_{in} = V_{DD}$, the output is some small V_{out} (V_{OL}) (Figure 2.29(c)). When $V_{in} = 0$, V_{out} rises to V_{DD}. As the resistor is made larger, the V_{OL} decreases and the current flowing when the inverter is turned on decreases. Correspondingly, as the load resistor is decreased in value, the V_{OL} rises and the ON current rises. Selection of the resistor value would seek a compromise between V_{OL}, the current drawn, and the pullup delay that increases with the value of the load resistor. Current sources have high output resistance and thus offer sharper transitions.

Neither high-value resistors nor ideal current sources are readily available in most CMOS processes. A more practical circuit called a *pseudo-nMOS inverter* is shown in Figure 2.30(a). It uses a pMOS transistor pullup or *load* that has its gate permanently grounded to approximate a constant current source. Pseudo-nMOS circuits get their name from the early nMOS technology (which preceded CMOS technology as a major systems technology) in which only nMOS transistors were available; the grounded pMOS transistor is reminiscent of a depletion mode nMOS transistor that is always ON.

The transfer characteristics may again be derived by finding V_{out} for which $I_{dsn} = |I_{dsp}|$ for a given V_{in}, as shown in Figure 2.30(b) and Figure 2.30(c). The beta ratio affects the shape of the transfer characteristics and the V_{OL} of the inverter. Larger pMOS transistors offer faster rise times but less sharp transfer characteristics. Figure 2.30(d) shows that when the nMOS transistor is turned on, a constant DC current flows in the circuit.

The gates in this section are called *ratioed* circuits because the transfer function depends on the ratio of the strength of the pulldown transistor to the pullup device. The resistor, current source, or ON transistor is sometimes called a *static load*. It is possible to construct other ratioed circuits such as NAND or NOR gates by replacing the pullup transistors with a single pullup device. Unlike complementary circuits, the ratio must be chosen so the circuit operates correctly despite any variations from nominal component values that may occur during manufacturing. Moreover, ratioed circuits dissipate power continually in certain states (e.g., when the output is low) and have poorer noise margins than complementary circuits.

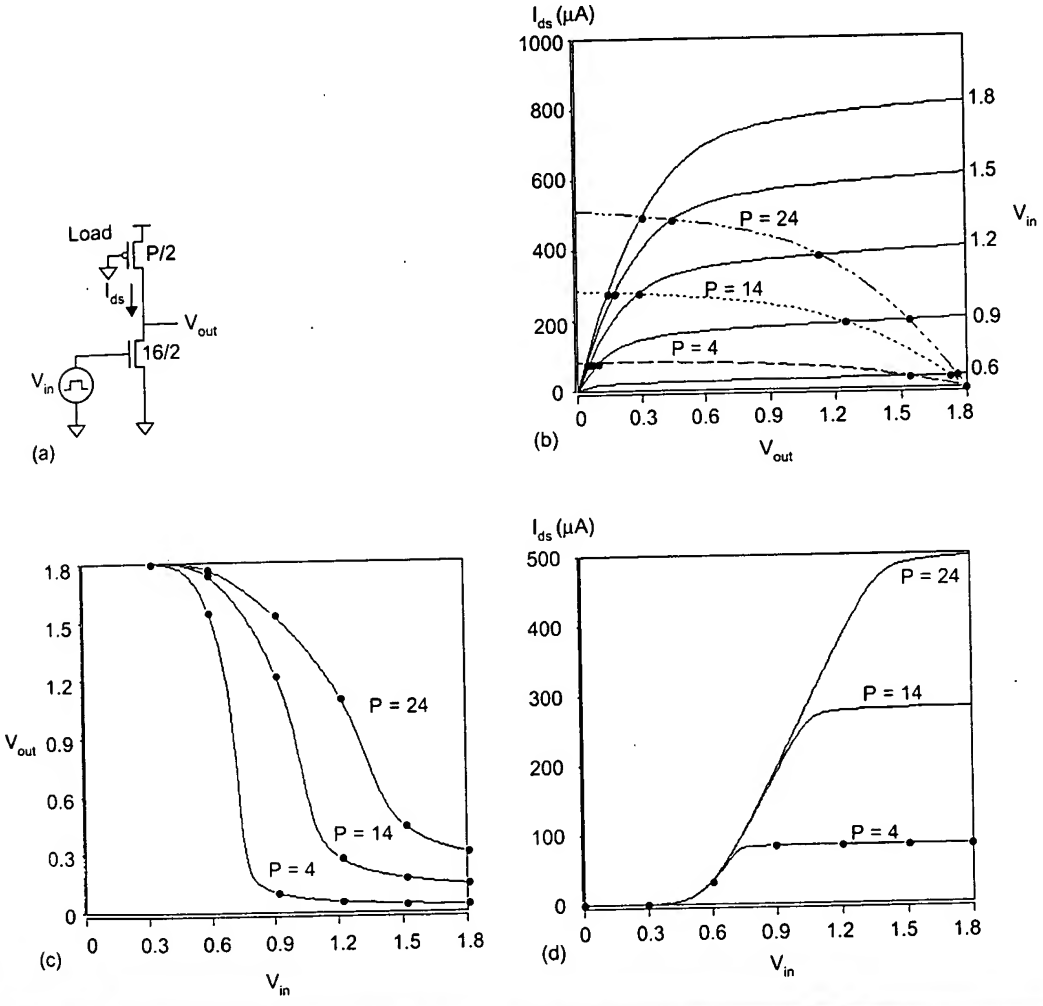

FIG 2.30 Pseudo-nMOS inverter and DC transfer characteristics

Therefore, ratioed circuits tend to be used only in very limited circumstances where they offer critical benefits such as smaller area or reduced input capacitance. We will return to ratioed circuits in Section 6.2.2.

2.5.5 Pass Transistor DC Characteristics

Recall from Section 1.4.6 that nMOS transistors pass '0's well but '1's poorly. We are now ready to better define "poorly." Figure 2.31(a) shows an nMOS transistor with the gate and drain tied to V_{DD}. Imagine that the source is initially at $V_s = 0$. $V_{gs} > V_{tn}$, so the transis-

Reducing the pMOS size from 2 to $\sqrt{2} \approx 1.4$ for the inverter gives the theoretical fastest average delay, but this delay improvement is only 2%. However, this significantly reduces the pMOS transistor area. It also reduces input capacitance, which in turn reduces power consumption. Unfortunately, it leads to unequal delay between the outputs. Some paths can be slower than average if they trigger the worst edge of each gate. Excessively slow rising outputs can also cause hot electron degradation. And reducing the pMOS size also moves the switching point lower and reduces the noise margin.

In summary, the *P/N* ratio of a library of cells should be chosen on the basis of area, power, and reliability, not average delay. For NOR gates, reducing the size of the pMOS transistors significantly improves both delay and area. In most standard cell libraries, the pitch of the cell determines the *P/N* ratio that can be achieved in any particular gate. Ratios of 1.5–2 are commonly used for inverters.

6.2.1.7 Multiple Threshold Voltages Some CMOS processes offer two or more threshold voltages. Transistors with lower threshold voltages produce more ON current, but also leak exponentially more OFF current. Libraries can provide both high- and low-threshold versions of gates. The low-threshold gates can be used sparingly to reduce the delay of critical paths [Kumar94, Wei98]. Skewed gates can use low-threshold devices on only the critical network of transistors.

6.2.2 Ratioed Circuits

Ratioed circuits, introduced in Section 2.5.4, use weak pull-up devices and stronger pull-down devices. They reduce the input capacitance and hence improve logical effort by eliminating large pMOS transistors loading the inputs, but depend on the correct ratio of pull-up to pull-down strength. If the pull-up is too strong, V_{OLmax} may be too high; V_{OLmax} is best chosen to be less than V_{tn} so the low output does not turn ON the next stage. If the pull-up is too weak, the rising delay will be too slow. Ratioed circuits also dissipate static power while the output is low, so they must be used in a limited fashion where they provide significant benefits.

6.2.2.1 Pseudo-nMOS Figure 6.12 shows *pseudo-nMOS* logic gates, which are the most common form of CMOS ratioed logic. The pull-down network is like that of a static gate, but the pull-up network has been replaced with a single pMOS transistor that is grounded so it is always ON. The pMOS transistor width is selected to be about 1/4 the strength (i.e., 1/2 the effective width) of the nMOS pull-down network as a compromise between noise margin and speed; this best size is highly process-dependent, but is usually in the range of 1/3 to 1/6.

To calculate the logical effort of pseudo-nMOS gates, suppose a complementary CMOS unit inverter delivers current *I* in both rising and falling transitions. For the widths shown, the pMOS transistors produce *I*/3 and the nMOS networks produce 4*I*/3. The logical effort for each transition is computed as the ratio of the input capacitance to that of a complementary CMOS inverter with equal current for that transition. For the

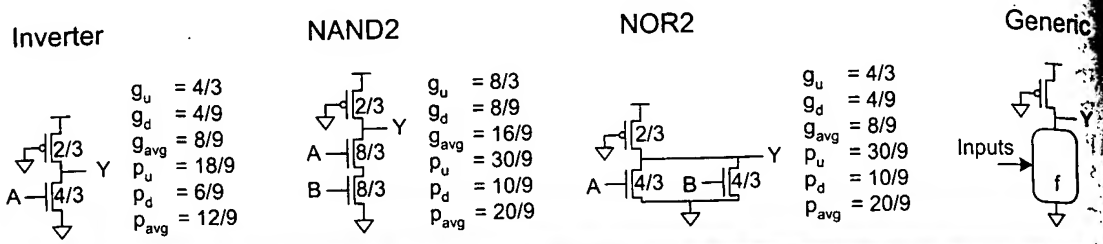

FIG 6.12 Pseudo-nMOS logic gates

falling transition, the pMOS transistor effectively fights the nMOS pull-down. The output current is estimated as the pull-down current minus the pull-up current, $(4I/3 - I/3) = I$. Therefore, we will compare each gate to a unit inverter to calculate g_u. For example, the logical effort for a falling transition of the pseudo-nMOS inverter is the ratio of its input capacitance (4/3) to that of a unit complementary CMOS inverter (3), i.e., 4/9. g_u is three times as great because the current is 1/3 as much.

The parasitic delay is also found by counting output capacitance and comparing it to an inverter with equal current. For example, the pseudo-nMOS NOR has 10/3 units of diffusion capacitance as compared to 3 for a unit-sized complementary CMOS inverter, so its parasitic delay pulling down is 10/9. The pull-up current is 1/3 as great, so the parasitic delay pulling up is 10/3.

As can be seen, pseudo-nMOS is slower on average than static CMOS for NAND structures. However, it works well for NOR structures. The logical effort is independent of the number of inputs in wide NORs, so pseudo-nMOS is useful for fast wide NOR gates or NOR-based structures like ROMs and PLAs when power permits.

Pseudo-nMOS gates will not operate correctly if $V_{OL} > V_{IL}$ of the receiving gate. This is most likely in the SF design corner where nMOS transistors are weak and pMOS transistors are strong. Designing for acceptable noise margin in the SF corner forces conservative choice of weak pMOS transistors in the normal corner. A biasing circuit can be used to reduce process sensitivity, as shown in Figure 6.15. The goal of the biasing circuit is to create a V_{bias} that causes *P2* to deliver 1/3 the current of *N2*, independent of the relative mobilities of the pMOS and nMOS transistors. Transistor *N2* has width of 3/2 and hence produces current $3I/2$ when ON. Transistor *N1* is tied ON to act as a current source with 1/3 the current of *N2*, i.e., $I/2$. *P1* acts as a current mirror using feedback to establish the bias voltage sufficient to provide equal current as *N1*, $I/2$. The size of *P1* is noncritical so long as it is large enough to produce sufficient current and is equal in size to *P2*. Now, *P2* ideally also provides $I/2$. In summary, when *A* is low, the pseudo-nMOS gate pulls up with a current of $I/2$. When *A* is high, the pseudo-nMOS gate pulls down with an effective current of $(3I/2 - I/2) = I$. To first order, this biasing technique sets the relative currents strictly by transistor widths, independent of relative pMOS and nMOS mobilities.

Example

Design a k-input AND gate with DeMorgan's Law using static CMOS inverters followed by a k-input pseudo-nMOS NOR, as shown in Figure 6.13. Let each inverter be unit-sized. If the output load is an inverter of size H, determine the best transistor sizes in the NOR gate and estimate the average delay of the path.

Solution: The path electrical effort is H and the branching effort is $B = 1$. The inverter has a logical effort of 1. The pseudo-nMOS NOR has an average logical effort of 8/9 according to Figure 6.12. The path logical effort is $G = 1 \cdot (8/9) = 8/9$, so the path effort is $8H/9$. Each stage should bear an effort of $\hat{f} = \sqrt{8H/9}$. Using the capacitance transformation gives NOR pull-down transistor widths of

$$C_{in} = \frac{gC_{out}}{\hat{f}} = \frac{(8/9)H}{\sqrt{8H/9}} = \frac{\sqrt{8H}}{3}$$

unit-sized inverters. As a unit inverter has three units of input capacitance, the NOR transistor nMOS widths should be $\sqrt{8H}$. According to Figure 6.12, the pull-up transistor should be half this width. The complete circuit marked with nMOS and pMOS widths is drawn in Figure 6.14.

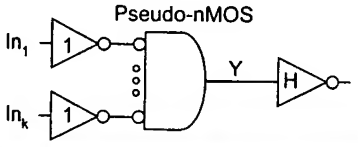

FIG 6.13 k-input AND gate driving load of H

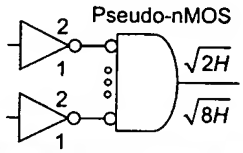

FIG 6.14 k-input AND marked with transistor widths

We estimate the average parasitic delay of a k-input pseudo-nMOS NOR to be $(8k + 4)/9$. The total delay in τ is

$$D = N\hat{f} + P = \frac{4\sqrt{2}}{3}\sqrt{H} + \frac{8k+13}{9}.$$

Increasing the number of inputs only impacts the parasitic delay, not the effort delay.

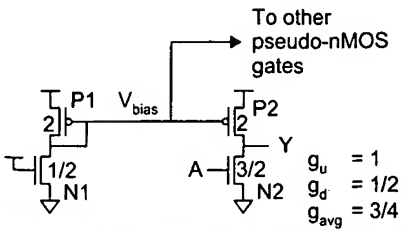

FIG 6.15 Replica biasing of pseudo-nMOS gates

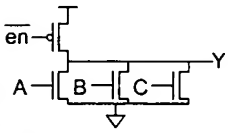

FIG 6.16 Pseudo-nMOS gate with enabled pull-up

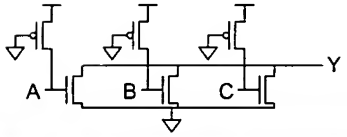

FIG 6.17 3-input NOR drawn as multidrain logic

Such replica biasing permits the 1/3 current ratio rather than the conservative 1/4 ratio in the previous circuits, resulting in lower logical effort. The bias voltage V_{bias} can be distributed to multiple pseudo-nMOS gates. Ideally, V_{bias} will adjust itself to keep V_{OL} constant across process corners. Unfortunately, the currents through the two pMOS transistors do not exactly match because their drain voltages are unequal, so this technique still has some process sensitivity. Also note that this bias is relative to V_{DD}, so any noise on either the bias voltage line or the V_{DD} supply rail will impact circuit performance.

Turning off the pMOS transistor can reduce power when the logic is idle or during IDDQ test mode (see Section 9.6.8), as shown in Figure 6.16.

An alternate way to represent the pseudo-nMOS gate is to draw the pull-up at the input and the pull-down transistors with open drains, as shown in Figure 6.17. Multiple gates are tied together in a "wired-OR" fashion. This representation is called *CMOS Multidrain Logic* by the inventors [Wu87], but offers no advantages over normal pseudo-nMOS circuits in modern CAD environments.

6.2.2.2 Ganged CMOS Figure 6.18 illustrates pairs of CMOS inverters ganged together. The truth table is given in Table 6.1, showing that the pair compute the NOR function. Such a circuit is sometimes called a *symmetric*[2] *NOR* [Johnson88], or more generally, *ganged CMOS* [Schultz90]. When one input is '0' and the other '1,' the gate can be viewed as a pseudo-nMOS circuit with appropriate ratio constraints. When both inputs are '0,' both pMOS transistors turn on in parallel, pulling the output high faster than they would in an ordinary pseudo-nMOS gate. Moreover, when both inputs are '1,' both pMOS transistors turn OFF, saving static power dissipation. As in pseudo-nMOS, the transistors are sized so the pMOS are about 1/4 the strength of the nMOS and the pull-down current matches that of a unit inverter. Hence,

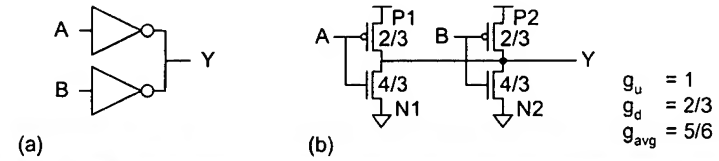

FIG 6.18 Symmetric 2-input NOR gate

[2]Do not confuse this use of *symmetric* with the concept of *symmetric* and *asymmetric* gates from Section 6.2.1.4.